REMARKS/ARGUMENTS

Applicant would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office Action, and amended as necessary to more clearly and particularly describe the subject matter which Applicant regards as the invention.

Claims 5, 10, and 14 have been amended. Claims 16-20 have been added.

The Examiner rejected claims 5, 7–9 and 15 under 35 U.S.C. 102(b) as being anticipated by Iida, U.S. Pat. No. 5,500,542. Iida does not teach all the limitations of claims 5, 7 and 9. More specifically, Iida does not teach "wherein at least one of the functional blocks has a logic circuit and a diode." Referring to column 8, lines 16–22 and to figure 2 of Iida, Iida discloses cells 31A to 31D which are considered functional blocks. The cells or functional blocks are connected by wiring. The wiring runs through the diodes D1 in the diode row 33X. The cells or functional blocks are merely connected to the diodes. Thus, the diodes are outside the cells or functional blocks. Thus, Iida does not teach where at least one functional block has a diode. Therefore Iida does not teach all the limitations of claims 7 and 9.

Claim 15 depends from claim 5 and claim 8 depends from claim 7, thus, all arguments pertaining to claims 5 and 7 are equally applicable to claims 15 and 8 and are herein incorporated by reference.

The Examiner rejected claim 6 under 35 U.S.C. 103(a) as being unpatentable over Iida, U.S. Pat. No. 5,500,542 in view of Spaanenberg, U.S. Pat. No. 4,656,592. Claim 6 depends from claim 5, thus, all arguments pertaining to claim 5 are equally applicable to claim 6 and are herein incorporated by reference.

The Examiner rejected claims 10–14 under 35 U.S.C. 103(a) as being unpatentable over Iida, U.S. Pat. No. 5,500,542 in view of Katsube, U.S. Pat. No. 5,828,119. Iida does not teach all the limitations of claims 10, 12 and 14. More specifically, Iida does not teach "wherein at

least one of the functional blocks has a logic circuit and a diode." Referring to column 8, lines 16–22 and to figure 2 of Iida, Iida discloses cells 31A to 31D which are considered functional blocks. The cells or functional blocks are connected by wiring. The wiring runs through the diodes D1 in the diode row 33X. The cells or functional blocks are merely connected to the diodes. Thus, the diodes are outside the cells or functional blocks. Thus, Iida does not teach where at least one functional block has a diode. Therefore Iida does not teach all the limitations of claims 12 and 14.

Claim 11 depends from claim 10 and claim 13 depends from claim 12, thus, all arguments pertaining to claims 10 and 12 are equally applicable to claims 11 and 13 and are herein incorporated by reference.

The cited prior art does not teach all the limitations of new claims 16-20. More specifically, the cited prior art does not teach "at least one functional block having a logic circuit and a diode."

In light of the foregoing, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No. 31638US4.

Respectfully submitted,

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